ABSTRACT OF THE DISCLOSURE:

A vector computer system includes a plurality of memory banks 40, a vector processor 11, and a plurality of additional processing units 30 each of which is connected to one of the memory banks 40. Each of the additional processing units 30 reads data from the corresponding memory bank 40 by referring to an address designated by the processor 11, and performs a designated operation about the data. Then the additional processing unit 30 stores the result of the operation into the designated address.